S_X_MPL Signal Acquisition Modeling and Processing Lab

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Channel Estimation with Reduced RF Chains

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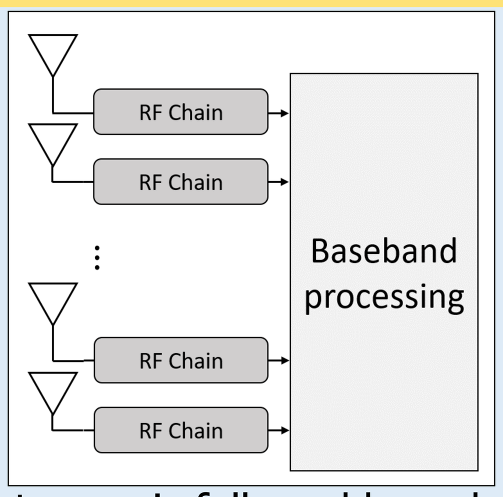
Main Contributions

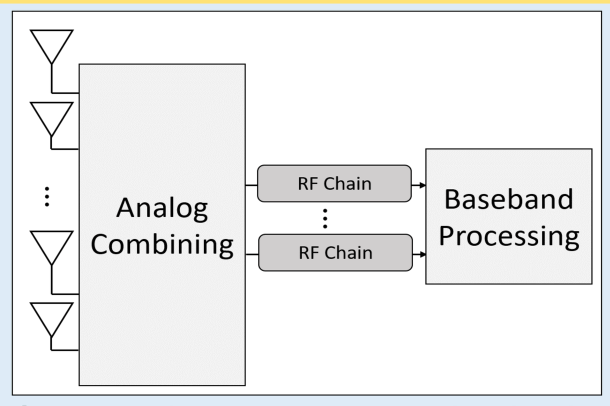
- This prototype demonstrates MIMO receiver with reduced number of RF chains
- Employs 4 antennas and only 2 RF chains
- Demonstrates an analog combiner that consists of controllable analog network of phase shifters, gains and switches
- Performs MMSE channel estimation for Kronecker channel model in a multi-user MIMO scenario
- When the channel matrix is low rank the RF reduction does not increase the channel's MSE

Conventional MIMO Receiver



- Each antennas is followed by a dedicated RF chain
- All the analog inputs from the antennas are accessible at the baseband
- All the signal processing operations are performed in baseband (fully-digital)

Hybrid MIMO Receiver



- An analog combiner projects the high number of analog inputs from the antennas onto the low number of RF chains
- The analog combiner consists of a controllable network of phase shifters, gains and switches
- Only a low number of measurements are accessible in baseband

Problem Formulation

- Multi-user MIMO scenario with 2 user terminals and a base station with 4 antennas and 2 RF chains
- The users transmit known, orthogonal pilot sequences of length τ to the base station, over a TDD uplink channel
- Received signal at the baseband

$$\boldsymbol{Y} = \boldsymbol{W}\boldsymbol{H}\boldsymbol{S}^T$$

(Received digital signal; Analog combiner matrix; Channel matrix; Pilot sequences matrix)

- Kronecker channel model:

$$\boldsymbol{H} = \boldsymbol{R}_r^{\frac{1}{2}}\bar{\boldsymbol{H}}\boldsymbol{R}_t^{\frac{1}{2}}$$

(Receive side correlation; White channel matrix with entries $\sim\mathcal{N}(0,1)$; Transmit side correlation)

- Vectorized received signal:

$$\boldsymbol{y} = (\boldsymbol{S}\otimes\boldsymbol{W})\,\boldsymbol{h} \sim \mathcal{N}(\boldsymbol{0}, \boldsymbol{R}_t\otimes\boldsymbol{R}_r)$$

- MMSE channel estimator

$$\hat{\boldsymbol{h}} = \left[\boldsymbol{R}_t\boldsymbol{S}^*\left(\boldsymbol{S}\boldsymbol{R}_t\boldsymbol{S}^*\right)^{-1}\otimes\boldsymbol{R}_r\boldsymbol{W}^*\left(\boldsymbol{W}\boldsymbol{R}_r\boldsymbol{W}^*\right)^{-1}\right]\boldsymbol{y}$$

Optimal Analog Combiner

- Due to the separable structure of the Kronecker model, an optimal analog combiner can be derived. [Stein and Eldar 2018]

$$\boldsymbol{W}_{opt} = \boldsymbol{T}\boldsymbol{U}_1^*$$

- $\boldsymbol{U}_1$ - First 2 eigenvectors of $\boldsymbol{R}_r$
- $\boldsymbol{T}$ - Any 2×2 invertible matrix

Theoretical MSE

- For the suggested combiner $\boldsymbol{W}_{opt}$ the theoretic MSE in a noise free scenario is the sum of 2 smallest eigenvalues of the receive-side correlation:

$$\mathbb{E}\left[\|\hat{\boldsymbol{H}}-\boldsymbol{H}\|^2\right] = \lambda_3(\boldsymbol{R}_r) + \lambda_4(\boldsymbol{R}_r)$$

- **Best case scenario:** $\mathrm{rank}(\boldsymbol{R}_r) \le 2$. In this case the MSE is:

$$\mathbb{E}\left[\|\hat{\boldsymbol{H}}-\boldsymbol{H}\|^2\right] = 0$$

- **Worst case scenario:** $\lambda_1(\boldsymbol{R}_r) = \lambda_2(\boldsymbol{R}_r) = \lambda_3(\boldsymbol{R}_r) = \lambda_4(\boldsymbol{R}_r) = a$. In this case the optimal combining scheme is a simple "antenna-selection" scheme, and the MSE is:

$$\mathbb{E}\left[\|\hat{\boldsymbol{H}}-\boldsymbol{H}\|^2\right] = 2a$$

Technical Specification

Carrier Frequency - f_c = 1GHz

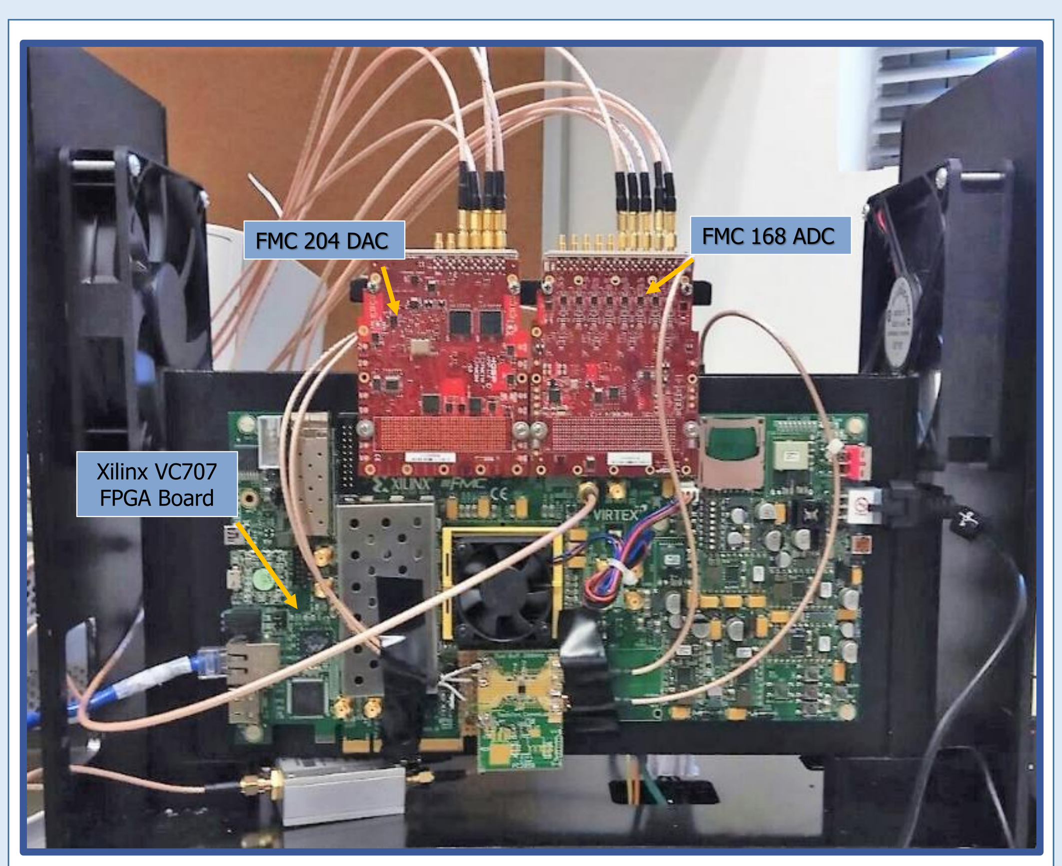
Baseband BW = 125MHz – can be extended up to 2GHz

DAC - 4 output channels at 250MSPS

ADC – 4 input channels
Sampling Rate – 250MHz for each channel

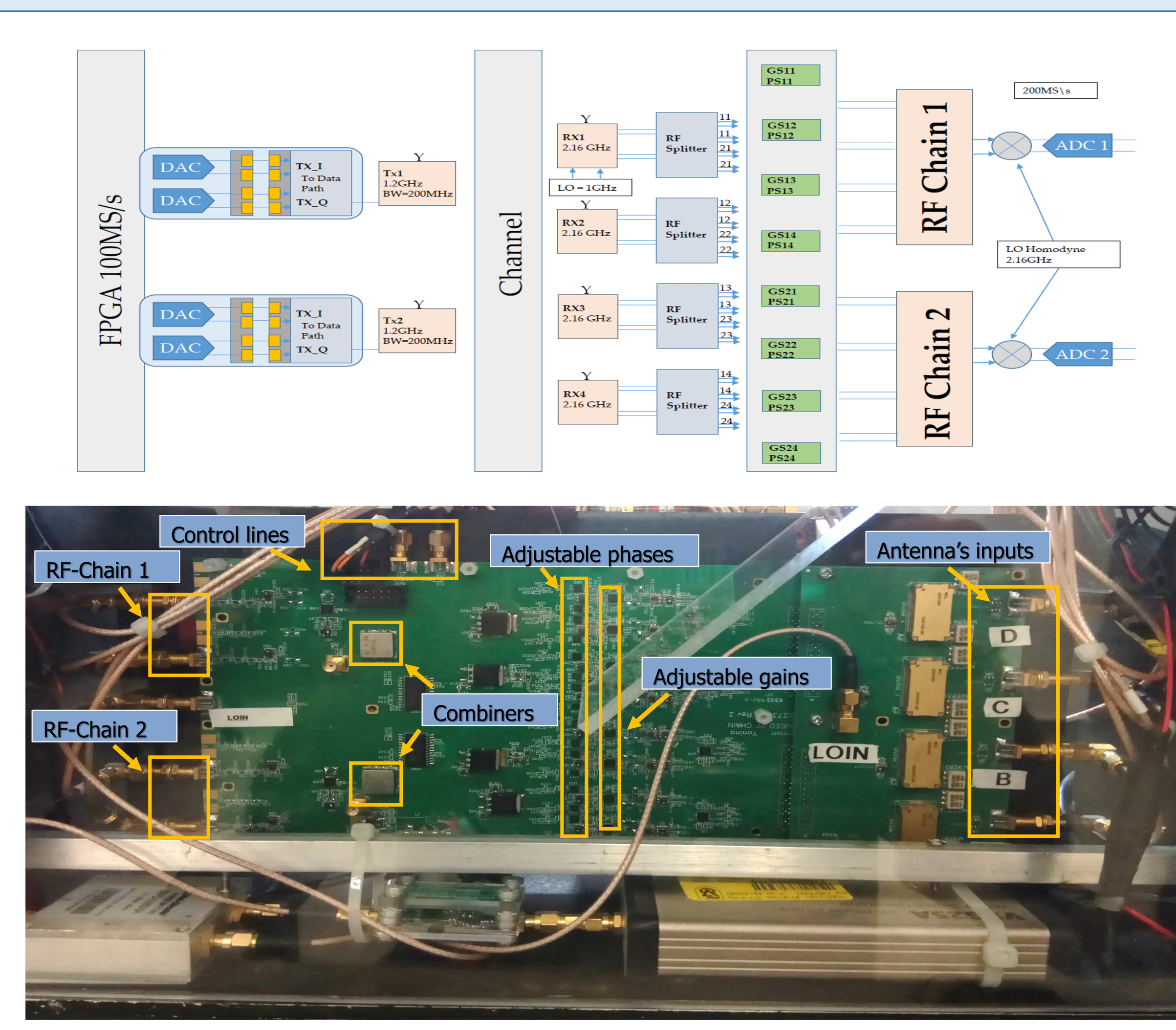
Digital Receiver and Waveform Generator

- 16-bit 8-channel digitizer for I and Q streams
- 16-bit 4-channel DAC for Waveform Generation
- Analog signal phase shift resolution - 0.5°
- Amplitude modulation

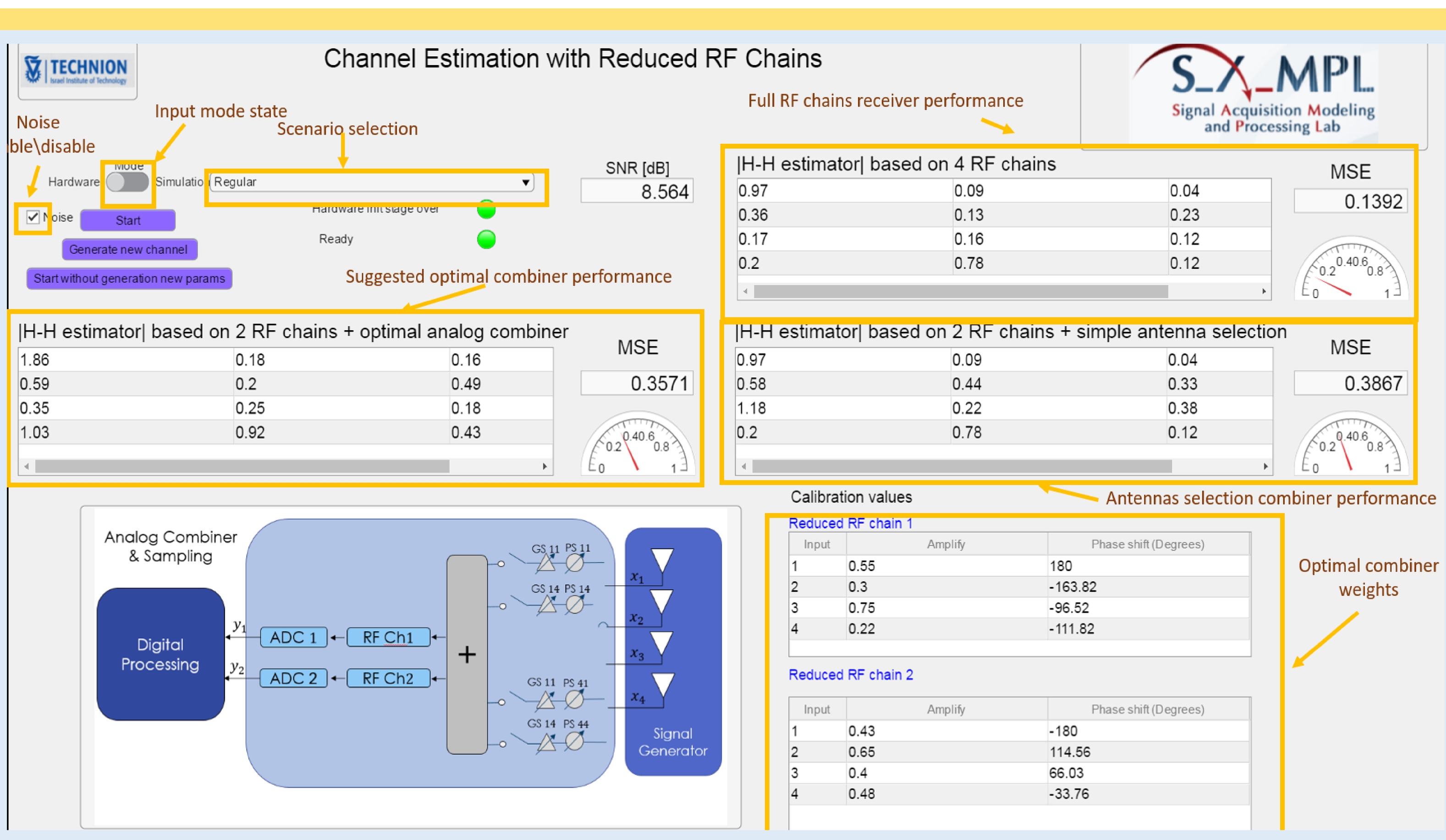


Analog Pre-Processor (APP)

- APP filters the received data coming from 4 input channels into 2 RF-Chains
- Phase and gain are easily configured by FPGA controller
- Each RF-Chain has 2 outputs: I and Q
- APP card is mounted on a single chassis



User Interface



Overview of Hardware Architecture