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Task-Based Low Bit Quantization for Channel Estimation Demo

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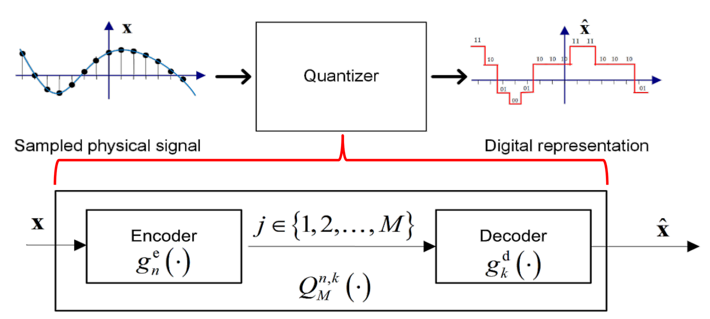
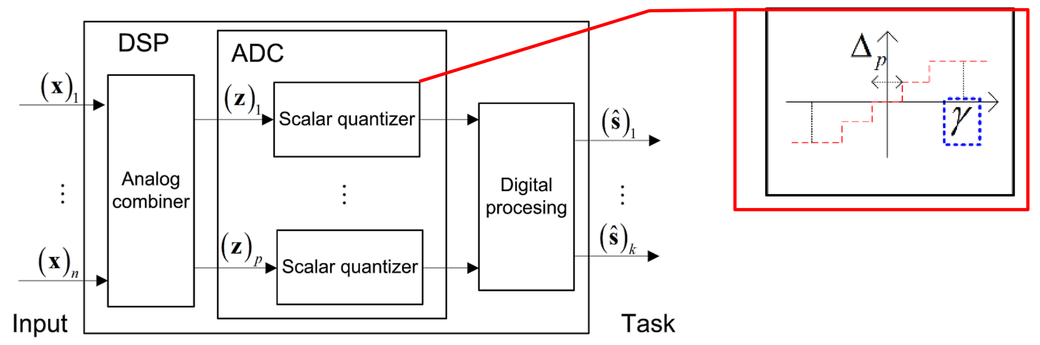
Motivation and Contributions

- Quantization allows representing of continuous-amplitude signals with discrete values
- Accurately representing signal requires huge quantization bits, which causes severe cost, power consumption, and memory burden
- We propose a task-based quantization approach implemented in hardware, which guarantees the recovery performance with low-bit representation
- The developed low-bit quantization board is applied to a specific task of channel estimation

Quantizer



(a) Conventional quantizer



(b) Task-based quantizer

- A quantizer consists of Encoder (analog→bits) and Decoder (bits →digital representation)
- Performance measures:

Quantization rate $R = \frac{1}{n}\log M$

Expected distortion $D = E\{\|x - \hat{x}\|^2\}$

- Simple scalar ADCs + Analog combiner
- Jointly optimize the combiner and the ADCs based on the task
- Task dimension $(k) \leq$ input dimension (n)

Problem Formulation

- For the task of finite inter-symbol interference (ISI) channel estimation, the parameter vector $\boldsymbol{s}$ represents the coefficients of a multipath channel with K taps. The received signal $\mathbf{x}$ has the following form:

$$(\boldsymbol{x})_i = \sum_{l=1}^{K} (\boldsymbol{s})_l a_{i-l+1} + w_i$$

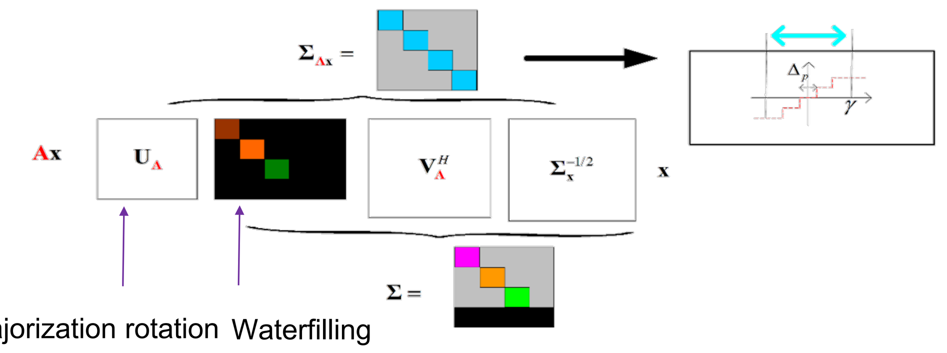
- Analog processing: $\boldsymbol{z} = \boldsymbol{A}\boldsymbol{x}$, with $\boldsymbol{A} \in \mathcal{R}^{P\times N}$ denoting the analog combiner
- Quantization and digital processing: $\hat{\boldsymbol{s}} = \boldsymbol{B}\boldsymbol{Q}(\boldsymbol{z})$, where $\boldsymbol{Q}(\cdot)$ denotes the low-bit quantization operation, and $\boldsymbol{B} \in \mathcal{R}^{K\times N}$ denotes the digital combiner
- The channel estimation distortion:

$$D = E\{\|\boldsymbol{s} - \hat{\boldsymbol{s}}\|^2\}$$

Task-Based Quantizer Design

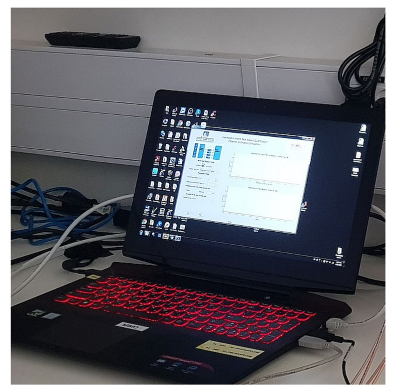
The optimal hardware-limited task-based quantizer includes[1]:

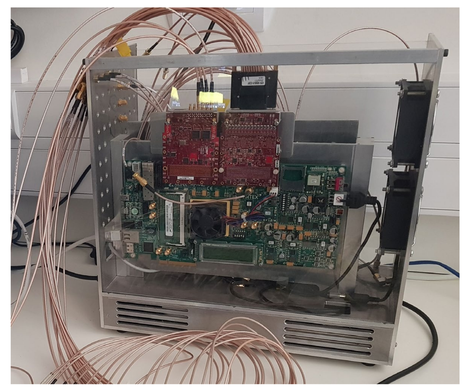
- Analog domain: "Waterfilling" + rotation
- Quantization: Overload free support
- Digital domain: MMSE estimation

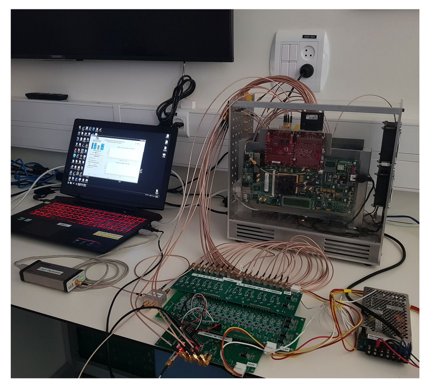


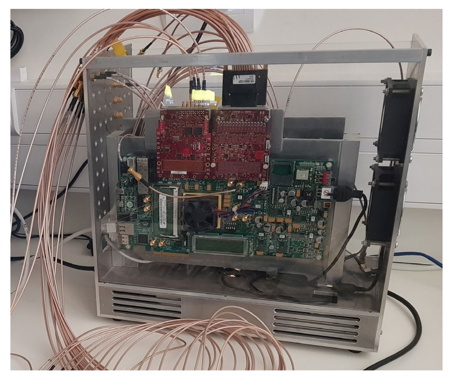
[1] N. Shlezinger, Y. C. Eldar, and M. R. Rodrigues, "Hardware-limited task-based quantization," IEEE Trans. Signal Process., vol. 67, no. 20, pp. 5223–5238, 2019.

Hardware

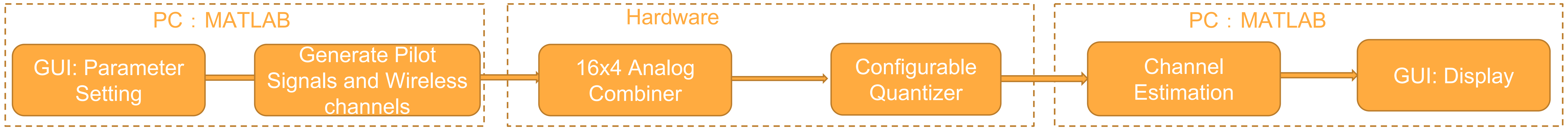




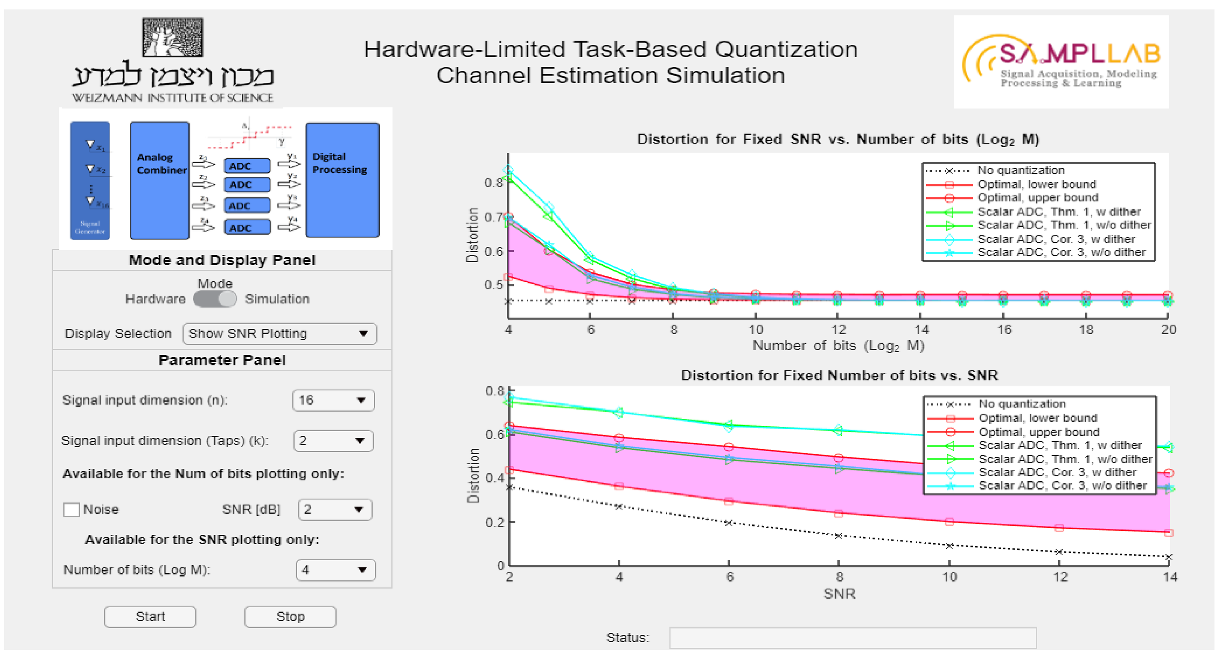




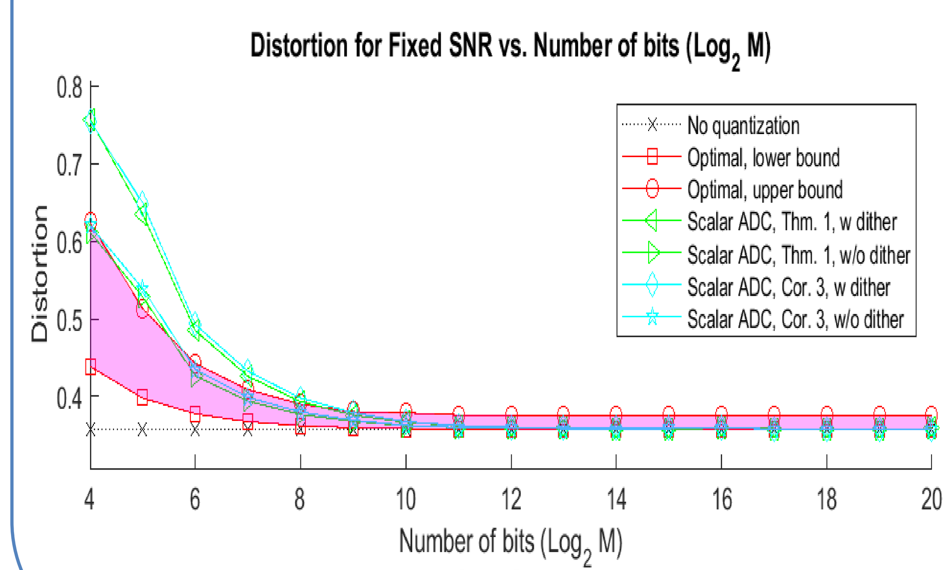
Parameters	Value
Carrier frequency	$f_c = 1$ GHz
Baseband bandwidth	$BW = 125$ MHz
DAC	4 channels, each $f_s = 125$MHz
ADC	4 channels, each 250 MSPS



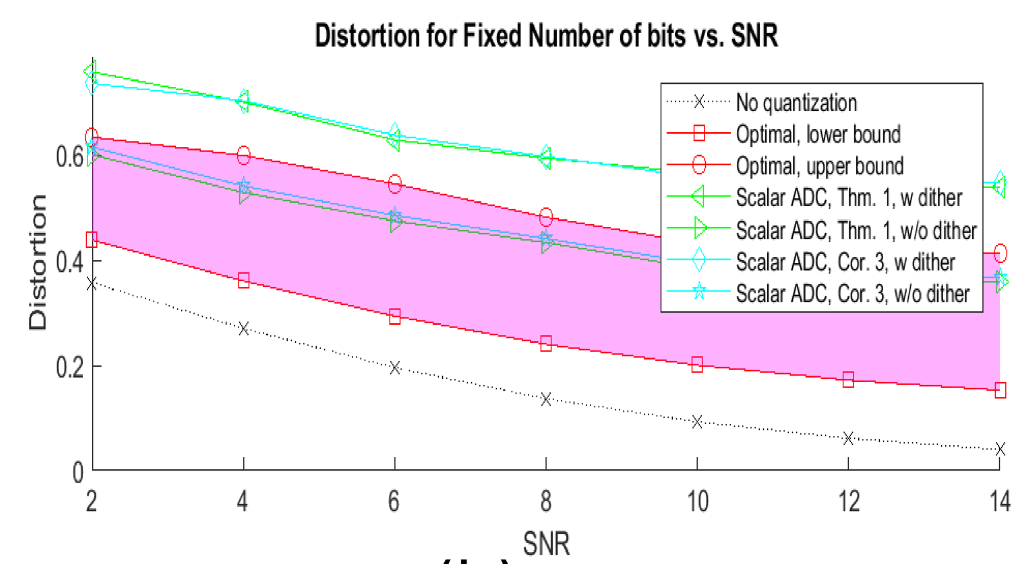
User Interface



Results



(a)



(b)

- We evaluate the achievable MSE in estimating a scalar ISI channel, using the developed hardware prototype. Figs (a) and (b) consider two different multipath channels with K=2 and K=8 taps, respectively
- From Figs (a) and (b), it can be observed that the proposed task-based low bit quantizer approaches the optimal performance as the quantization bit M increases.
- When each scalar quantizer uses at least five bits, i.e., $\log(M) \geq 5K$, the quantization error becomes negligible.